AMENDMENTS TO THE CLAIMS

Claims 1-4. (Cancelled)

5. (Currently Amended) A power MOSFET packaged device comprising:

a power MOSFET ~~according to claim 1~~ comprising:

a semiconductor substrate having one of main surface and the other main surface opposite to each other, the semiconductor substrate having a source electrode and a gate electrode provided on the one main surface and a drain electrode provided on the other main surface;

a source terminal layer disposed on the one main surface and joined to the source electrode;

a gate terminal layer disposed on the one main surface and joined to the gate electrode; and

a drain terminal layer disposed on the other main surface and joined to the drain electrode;

wherein the source terminal layer and the gate terminal layer are respectively disposed on the one main surface with such sizes as to fall within the area of the one main surface, and the drain terminal layer is disposed with such a size as to fall within the area of the other main surface, and

a circuit board, wherein

the power MOSFET is packaged in such a manner that the respective main surfaces of the semiconductor substrate in the power MOSFET are substantially normal to a circuit board.

6. (Original) The power MOSFET packaged device according to claim 5, wherein the source terminal layer, the gate terminal layer, and the drain terminal layer in the power MOSFET are respectively brazed to the circuit board with brazing materials.

7. (Original) The power MOSFET packaged device according to claim 5, wherein an encapsulating resin material is provided so as to cover the semiconductor substrate, the source terminal layer, the gate terminal layer, and the drain terminal layer in the power MOSFET.

8. (Withdrawn) A method of manufacturing a plurality of power MOSFETs, comprising the steps of:

preparing a semiconductor wafer including a plurality of power MOSFETs each having a semiconductor substrate, a source electrode and a gate electrode on one main surface of the semiconductor substrate and a drain electrode on the other main surface thereof;

forming a first terminal board contacting in common with the source electrode and the gate electrode of said each power MOSFET contained in the semiconductor wafer and forming a second terminal board contacting in common with the drain electrode of said each power MOSFET contained in the semiconductor wafer; and

dividing the semiconductor wafer in association with the power MOSFETs and thereby constituting the power MOSFETs each having, on the one main surface side of the semiconductor substrate, a source terminal layer and a gate terminal layer respectively brought into contact with the source electrode and the gate electrode, and having, on the other main surface side, a drain terminal layer brought into contact with the drain electrode.

9. (Withdrawn) The method according to claim 8, further comprising a terminal board shaping step after the terminal board forming step, wherein, in the terminal board shaping step, the first terminal board is shaped into a pattern in which the source terminal layers respectively corresponding to the source electrodes of said individual power MOSFETs and the gate terminal layers respectively corresponding to the gate electrodes thereof are connected to one another by slender connecting pieces, and the second terminal board is shaped into a pattern in which the drain terminal layers respectively corresponding to the drain electrodes of said individual power MOSFETs are connected to one another by slender connecting pieces.

10. (Withdrawn) The method according to claim 9, further comprising a brazing layer forming step after the terminal board shaping step, wherein, in the brazing layer forming step, the respective source terminal layers, gate terminal layers, and drain terminal layers and the connecting pieces are plated with brazing layers respectively.

11. (Withdrawn) The method according to claim 10, wherein the dividing step is executed after the brazing layer forming step.

12. (Withdrawn) A method of manufacturing a plurality of power MOSFETs, comprising the steps of:

preparing a semiconductor wafer including a plurality of the power MOSFETs each having a semiconductor substrate, a source electrode and a gate electrode on the side of one main surface of the semiconductor substrate and a drain electrode on the side of the other main surface thereof;

forming source terminal layers, gate terminal layers, and drain terminal layers, after the wafer preparing step, by evaporating a metal layer onto the source electrodes, gate electrodes, and drain electrodes of the respective power MOSFETs contained in the semiconductor wafer; and

dividing the semiconductor wafer, after the terminal layer forming step, in association with the respective power MOSFETs to thereby constitute the individual power MOSFETs.